Attorney Docket No.: 0254-094-CIP4-C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Memory Expansion and Chip Scale Stacking System and Method

Application No.:

10/814,530

Filing Date:

03/31/2004

Inventor:

Russell Rapport, et al.

Assignee:

Staktek Group, L.P.

Examiner:

TBA

Group:

TBA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

Pursuant to the guidelines for Information Disclosure Statements, 37 C.F.R. §§ 1.97-1.98, attached hereto is PTO Form 1449 (six sheets) with references listed for consideration by the Office.

In accordance with 37 C.F.R. § 1.98(a), copies of the listed written references are being provided.

In accordance with 37 C.F.R. §§ 1.97(g)-(h), the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b) or prior art under 35 U.S.C. §§ 102 or 103.

This Information Disclosure Statement is being filed before receipt of the first Office action, so no fee is believed to be due. The Commissioner is hereby authorized to charge any fees which may be required in connection with the filing, or to credit any overpayment to Deposit Account No. 50-0897, upon which account the undersigned has the authority to sign. A duplicate copy of Form 1449 is enclosed.

Respectfully submitted,

ANDREWS & KURTH LI

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April (92004)

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*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICANT

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